May, 2023

Join a fast-moving health focused technology company creating simple, smart and personalized wearables designed to help individuals on their health journey optimize for good health today and to help prevent and manage chronic diseases in the future.

Movano Health, a publicly traded startup company (NASDAQ:MOVE) headquartered in Pleasanton California is developing a suite of purpose-driven healthcare solutions to bring medical-grade, high-quality data to the forefront of consumer health devices. Featuring modern form factors, Movano Health's devices capture a comprehensive picture of a person's vital health information and uniquely translate the data into personalized and intelligent insights that empower consumers to live healthier and more balanced lives. Movano Health's end-to-end solutions will soon enable consumers, caretakers, and healthcare professionals to utilize daily medical-grade data as a tool to proactively monitor and manage their health. For more information on Movano Health, visit https://movanohealth.com/ .

Movano Health's Evie Ring, which is specifically designed to address women's health concerns, will be available for purchase in mid-2023. To stay up to date on Evie's launch, visit https://eviering.com/.

We are developing a proprietary platform that uses a custom SoC with mmWave RF technology for blood pressure and continuous non invasive Glucose measurements. Movano Health's Irish subsidiary is leading this IC development.

We require an ASIC/SoC digital verification Engineer with a whole system view to work on innovative SoCs in highly advanced process nodes.

The ideal applicant will have an MSEE with 2+ years of ASIC verification experience.

Responsibilities:

- Work with the design team to define the verification requirements.
- Develop test plans from a specification document.
- Write UVM verification test bench architecture, agents, and test sequences.
- Review test plans and verification code.
- Implement SVA for functional and formal verification.
- Implement coverage and review coverage results.
- Responsible for the verification of digital designs in complex Mixed-Signal chips.

Qualifications and Requirements:

- 2 plus years of experience as a verification engineer with successful Tape-outs
- Experience in architecting and developing testbenches and verification components like bus functional models and scoreboards/checkers.
- 2 plus years of industry experience in verifying complex designs both at the component and full-chip level.
- Experience in System Verilog based OVM / UVM, VMM or related object oriented and coverage driven ASIC verification methodology.

- Verification test planning, test bench architecture, assertions, problem solving and debug
- Programming skills such as Verilog or VHDL, C/C++, Tcl/Perl/Python/shell-scripting.
- The ability to work autonomously, precisely, and to drive innovation
- Good communication skills.

We're looking for people with strong multi-functional collaboration capability who are self-motivated and proactive.

You will be located in our European HQ in Cork, Ireland. Partial remote working can be accommodated.

Competitive compensation package including bonus and stock options with a comprehensive benefits package including medical insurance and pension.