Department of Electronic and Computer Engineering

UNIVERSITY OF LIMERICK
OLLSCOIL LUIMNIGH

Midas/Skillnet CPD Course
Digital Test and Measurement
Autumn semester 2024

Introduction

This document provides a summary of the Midas/Skillnet Continuing Professional Development (CPD) course in *Digital Test and Measurement*.

This 15-week CPD module will have a specific focus towards digital Integrated Circuit (IC) and system test. The role of the test engineer is becoming ever more diverse with activities that link into design and IC fabrication. In this course, the role of test and test development engineering will be introduced and discussed in relation to their integration within a modern semiconductor company. The actions undertaken within the role of test will be discussed, and the types of tests undertaken to identify the operation of digital ICs will be elaborated.

A 1-hour online orientation session will be provided in week 0 but the course formally will commence in week 1 with a 1-day on-campus session followed by 11 weeks of online learning through lectures, laboratories, and tutorial sessions. There will be 2 weeks of project work followed by a 1-day on-campus session for project presentation and course assessment in week 15.

Weeks	Activity	Dates
0	Orientation week	02 Sep 2024 to 06 Sep 2024
1 to 12	Teaching weeks	09 Sep 2024 to 29 Nov 2024
13	Reading (revision) week	02 Dec 2024 to 06 Dec 2024
14 to 15	Examination weeks	07 Dec 2024 to 21 Dec 2024

Notes

1. All on-campus activities will be undertaken in the University of Limerick Main Building, laboratory number B2-043
2. All online activities will be undertaken using Brightspace: https://learn.ul.ie/
3. Online sessions will be recorded and available for viewing during the operation of the module.
4. University of Limerick campus maps: https://www.ul.ie/buildings/campus-maps
5. University of Limerick car parks: https://www.ul.ie/buildings/parking

Computing requirements

Participants will require a laptop computer with a minimum of 16 GBytes RAM and two available USB ports. The software to install can be downloaded (free) and will be:

AMD (Xilinx) Vivado

- AMD (Xilinx) Vivado will be required for Verilog HDL design module creation and testfixture module simulation.
- Programming the FPGA each time the experiment is run. FPGA programming will be undertaken using a Tcl script and configuration data files provided. However, this requires Vivado to be installed as programming the FPGA uses Vivado files.

Verilog-HDL

- Verilog HDL will be used to enter a digital design (combinational logic, synchronous sequential logic, memory (RAM and ROM)), and simulate the design using a Verilog HDL testfixture. The test patterns generated will be stored in a text file that will be used to apply to physical hardware.

Python

- The Python language will be used to create scripts that communicate with the FPGA board, send commands and data to the microprocessor programmed into the FPGA, and receive experiment results from the microprocessor.

PyCharm

- Python scripts will be written and run using the PyCharm Integrated Development Environment (IDE).

Digilent Waveforms

- Waveform viewing software for the Digilent Analog Discovery.

Timetable

The module will run from September to December 2024 as follows:

Teaching week	Date and time	Location	Lecture	Laboratory	Tutorial	Notes
0	Wednesday 4th September 4:00 – 5:00 pm	Online				MS Teams. Meeting invitation will be sent out to participants in the week before the meeting.
1	Wednesday 11th September 10:00 am – 4:15 pm	On-campus	1 & 2	1	1	Physical meeting on the University of Limerick campus. Experiment hardware kits will be distributed.
2	Wednesday 18th September 1:30 - 6:00 pm	Online	3 & 4	2	2	Sessions will be undertaken using the Brightspace Virtual Learning Environment (VLE) and BigBlueButton (BBB).
3	Wednesday 25th September 1:30 - 6:00 pm	Online	5 & 6	3	3	
4	Wednesday 2nd October 1:30 - 6:00 pm	Online	7 & 8	4	4	
5	Wednesday 9th October 1:30 - 6:00 pm	Online	9 & 10	5	5	
6	Wednesday 16th October 1:30 - 6:00 pm	Online	11 & 12	6	6	
7	Wednesday 23rd October 1:30 - 6:00 pm	Online	13 & 14	7	7	
8	Wednesday 30th October 1:30 - 6:00 pm	Online	15 & 16	8	8	
9	Wednesday 6th November 1:30 - 6:00 pm	Online	17 & 18	9	9	
10	Wednesday 13th November 1:30 - 6:00 pm	Online	19 & 20	10	10	
11	Wednesday 20th November 1:30 - 6:00 pm	Online	21 & 22	11	11	
12	Wednesday 27th November 1:30 - 6:00 pm	Online	23 & 24	12	12	
13	Wednesday 4th December 4:00 – 5:00 pm	Online		Project		
14	Wednesday 11th December 4:00 – 5:00 pm	Online		Project		
15	Wednesday 18th December 10:00 am – 4:15 pm	On-campus				Physical meeting on the University of Limerick campus. End-of-Semester test and project demonstration. Submission of project report and design code. Experiment hardware kits will be returned.

Lecture timetable

Week	First lecture theme	Second lecture theme
1	Overview of test engineering activities	Fabrication processes, defects, and faults
2	Functional and structural tests	Test pattern generation (TPG)
3	Combinational logic test	Combinational logic test
4	Synchronous sequential logic test	Synchronous sequential logic test
5	Core and Periphery cells	Core and Periphery cells
6	Automatic Test Equipment (ATE) support	Automatic Test Equipment (ATE) support
7	Design for Testability (DfT)	Design for Testability (DfT)
8	Design for Testability (DfT)	IEEE standards
9	Memory test (ROM)	Memory test (ROM)
10	Memory test (RAM)	Memory test (RAM)
11	Built-In Self-Test - Logic (LBIST)	Built-In Self-Test - Logic (LBIST)
12	Built-In Self-Test - Memory (MBIST)	Built-In Self-Test - Memory (MBIST)

Laboratory timetable

Week	Laboratory theme
	Xilinx Vivado: Verilog HDL design module and testfixture experiments
1	Introduction and setting-up the experiments. Combinational logic circuit 1 design entry and simulation.
2	Combinational logic circuit 2 design entry and simulation.
3	Synchronous sequential logic circuit 1 design entry and simulation.
4	Synchronous sequential logic circuit 2 design entry and simulation.
5	Memory circuit 1 (ROM: Read Only Memory) design entry and simulation.
6	Memory circuit 2 (RAM: Random Access Memory) design entry and simulation.
	FPGA and Python based hardware experiments
7	Combinational logic circuit 1 test.
8	Combinational logic circuit 2 test.
9	Synchronous sequential logic circuit 1 test.
10	Synchronous sequential logic circuit 2 test.
11	Memory test: ROM and RAM.
12	Project planning and project set-up. Basic test of the Circuit Under Test (CUT).
13	UNDERTAKE PROJECT
14	UNDERTAKE PROJECT
15	Project demonstration and report submission

Tutorial timetable

Week	Tutorial theme
	Xilinx Vivado: Verilog HDL design module and testfixture experiments
1	Introduction and setting-up the experiments. Combinational logic circuit 1 design entry and simulation.
2	Combinational logic circuit 2 design entry and simulation.
3	Synchronous sequential logic circuit 1 design entry and simulation.
4	Synchronous sequential logic circuit 2 design entry and simulation.
5	Memory circuit 1 (ROM: Read Only Memory) design entry and simulation.
6	Memory circuit 2 (RAM: Random Access Memory) design entry and simulation.
	FPGA and Python based hardware experiments
7	Combinational logic circuit 1 test.
8	Combinational logic circuit 2 test.
9	Synchronous sequential logic circuit 1 test.
10	Synchronous sequential logic circuit 2 test.

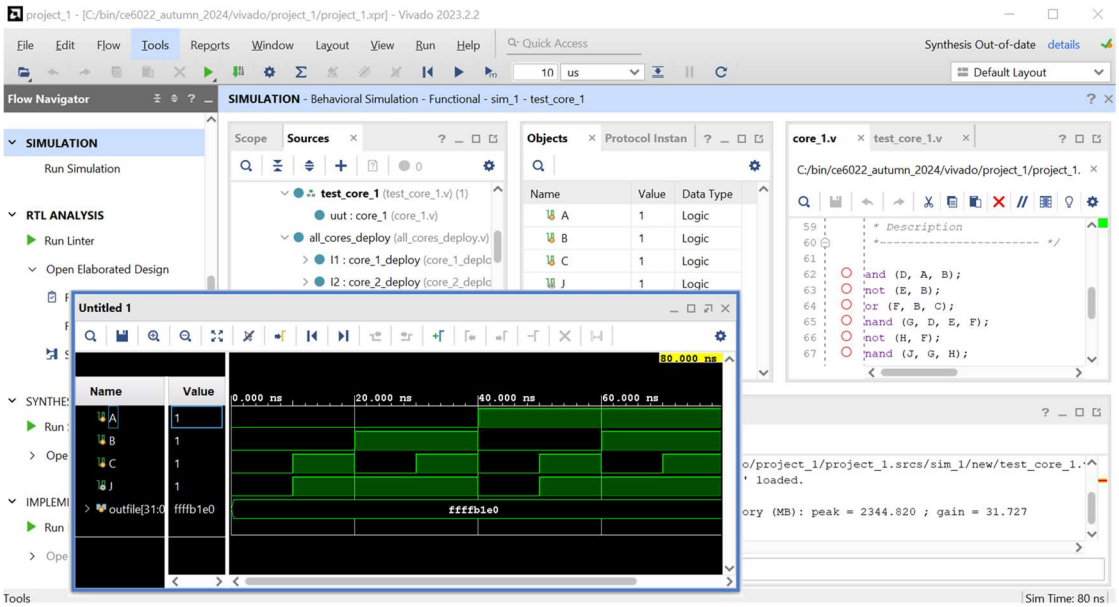
11	Memory test: ROM and RAM.
12	Project planning and project set-up. Basic test of the Circuit Under Test (CUT).

Laboratory Experiments

12 weeks laboratories and 3 weeks project. The laboratories will be based on 2 parts with Stuck-At-Fault (SAF) insertion in specific circuits:

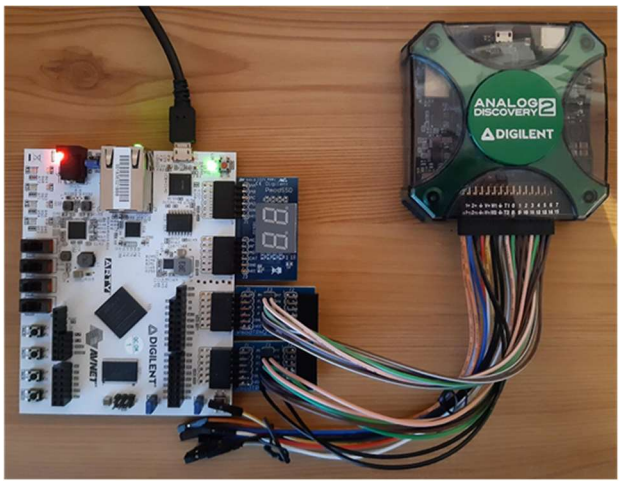
Part 1

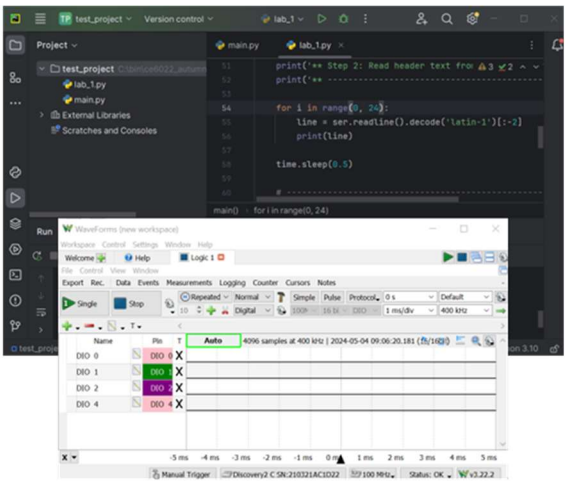
- Design entry, design interpretation, simulation, file I/O (test pattern file generation). SAF insertion. Scan path test insertion.



Part 2

- Test program development, Test pattern from part 1 used on hardware. SAF insertion. Logic signal monitoring using the Digilent Analog Discovery.





Verilog HDL design modelling and simulation: Xilinx Vivado. Appreciate design aspects with a focus on test.

Hardware implementation testing using Xilinx FPGA logic signal monitoring. Python/PyCharm computer interfacing. Digilent Waveforms. Test program development and application.