The emergence of Internet of Things (IOT) and cloud computing has triggered a rapid increase in bandwidth demand in data centers and telecommunication infrastructures, prompting the industry to propose a new electrical interface standard capable of operating up to 56Gb/s per-lane over a legacy channel built for lower data-rate. This presentation discusses the design of a 56Gb/s ADC-based PAM4 transceiver with a moderate target BER (e.g. 1e-6 to 1e-8) over legacy channels to be used with Forward Error Correction (FEC). Architecture and circuit solutions to address transmitter and receiver design challenges will be covered, as well as measurement results from a test-chip implemented in 16nm FinFET.

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